Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
655 EXTENDED INSTRUCTION SET PROCESSOR

No. 43A232719

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2.4.1 Configuration and Conditions

The assumed 6000 configurations for each set of instruction execution times are as follows:

1) A 6040 Processor on one 6000 System Controller with one 1.2 microsecond store.

2) A 6060 Processor with one 6000 System Controller with two 1.2 microsecond stores. This configuration does not have interlacing between store units and the system controller.

3) A 6060 Processor with one 6000 System Controller with two 1.2 microsecond stores. This configuration has interlacing between store units and the system controller.

4) A 6080 Processor with one 6000 System Controller with two 0.5 microsecond stores. This configuration does not have interlacing between store units and the system controller.

5) A 6080 Processor with two 6000 System Controllers with two 0.5 microsecond stores on each. This configuration has interlacing between store units and between system controllers.

Interlaced operation allows both controllers and/or store systems to be running simultaneously. The instructions are fetched in pairs and the operands are fetched individually. The following assumptions were used in arriving at the execution times:

1) A best case instruction operand distribution exists between the two stores, such that all access requests alternate between stores.

2) The instructions are fetched in pairs and the operands start on double word boundaries.

3) There are no interfering devices.

4) Cable length of 10 feet is used.

5) There is no indirect addressing, no scaling, no rounding, no truncation, and no overflow.

2.4.2 Address Modification Times

Index register, direct upper, and direct lower address modifications shall have no effect on instruction execution times. Address modifications utilizing an address register shall not increase instruction execution time more than 100 nanoseconds each time an address register modification is specified. For indirect address modification, the instruction execution times shall be modified for each level of indirectness by no more than the maximum values shown in Table 2.4.2.

INSTRUCTION TYPE	CONFIGURATIONS (See 2.4.1)				
	1	2	3	4	5
	6040	6060		6080	
Basic Add, Subtract, Load, Store	3.0	1.9	1.4	1.0	.7
Indexing	0.0	0.0	0.0	0.0	0.0
Fixed Point Multiply	13.5	3.6	3.6	3.5	3.6
Program Transfer	1.8	1.8	1.8	1.3	1.2
Shift 6 Bits	3.5	1.4	1.3	1.1	1.0
Fixed Point Divide	25.7	7.3	7.3	7.3	7.3
Floating Add, Subtract	5.3	1.8	1.8	1.2	1.2
Floating Multiply	11.8	3.1	3.1	3.1	3.1
Floating Divide	26.4	7.5	7.5	7.5	7.5
Move 9-9 (5 Char)	10.5	8.7	8.7	4.2	4.2
Move 6-6 (5 Char)	13.0	10.0	10.0	6.1	6.1
Edit Move (5 digits + sign) (MOPs - CHT,MSES)	16.5	13.7	11.9	10.5	10.5
Alpha Compare (five 6-bit)	8.8	7.5	7.5	4.6	4.6
Numeric Compare (five 4-bit)	7.0	6.0	6.0	4.0	4.0
Decimal Add, Subtract (five 4-bit)	11.0	8.2	8.2	5.0	5.0
Decimal Multiply (five 9-bit x five 9-bit)	18.1	14.8	14.8	10.8	10.8
Decimal Divide (ten 9-bit ÷ five 9-bit)	23.9	20.6	20.6	16.2	16.2

INSTRUCTION EXECUTIONS TIMES

Table 2.4.1

MODIFICATION TYPE	0.5 MICROSECOND STORE	1.2 MICROSECOND STORE
RI	1.3	2.0
IR	1.3	2.0
IT with restoring of the indirect word	2.6	4.0
IT with no restoring of the indirect word	1.3	1.3

ADDRESS MODIFICATION TIMES

Table 2.4.2

	000(1)*	040(1)	100(1)	140(1)	200(1)	240(1)	300(1)	340(1)
000			MLR				MVN	
001			MRL				BTD	
002					AD2D			
003					SB2D		CMPN	
004								
005							DTB	
006			CMPC		MP2D			
007					DV2D			
010								
011								
012								
013								
014								
015								
016								
017								
020	MVE	CSL	SCD	MVT				
021		CSR	SCDR					
022					AD3D			
023					SB3D			
024	MVNE	SZTL	SCM	TCT				
025		SZTR	SCMR	TCTR				
026		CMPB			MP3D			
027					DV3D			
030								
031								
032								
033								
034								
035								
036								
037								

*See 3.3.2 for code representation

Figure 3-2a. Upper Half of Operation Code Map for the Extended Instructions

	400(1)*	440(1)	500(1)	540(1)	600(1)	640(1)	700(1)	740(1)
000			A9BD	ARA0	TRTN	ARN0		SAR0
001			A6BD	ARA1	TRTF	ARN1		SAR1
002			A4BD	ARA2		ARN2		SAR2
003		SAREG	ABD	ARA3		ARN3		SAR3
004				ARA4	TMOZ	ARN4		SAR4
005				ARA5	TPNZ	ARN5		SAR5
006				ARA6	TTN	ARN6		SAR6
007		SPL	AWD	ARA7		ARN7		SAR7
010								
011								
012								
013								
014								
015								
016								
017								
020			S9BD	AAR0		NAR0		LAR0
021			S6BD	AAR1		NAR1		LAR1
022			S4BD	AAR2		NAR2		LAR2
023		LAREG	SBD	AAR3		NAR3		LAR3
024				AAR4		NAR4		LAR4
025				AAR5		NAR5		LAR5
026				AAR6		NAR6		LAR6
027		LPL	SWD	AAR7		NAR7		LAR7
030								
031								
032								
033								
034								
035								
036								
037								

*See 3.3.2 for code representation.

Figure 3-2b. Lower Half of Operation Code Map for the Extended Instructions

3.3.3 Description of Modification Fields (continued)

**Except in the cases of A and Q, when a string length is contained in a register, the full 18 bits shall be interpreted as an index. Lengths in A or Q shall utilize the same number of bits as stated above for the REG field of an MF.

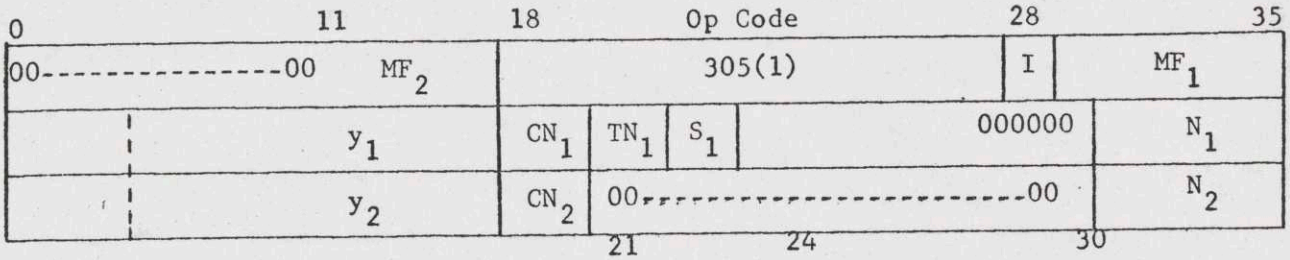
1) Specifying DU type address modification in the REG field of an Indirect Operand Descriptor shall be illegal and shall cause an IPR fault.

2) The contents of the IC shall always be interpreted as a word address when used in address modification. During the entire execution of a multi-word instruction, the IC points to the instruction word. Thus, if IC address modification is involved with a descriptor word, the instruction word address shall be used.

3.4.4 Conversion Instructions

These instructions are used for conversions between binary and decimal numbers where the binary number is stored as a character string, starting and ending on 9-bit character boundaries, and the decimal number is stored as a character string.

DTB Decimal to Binary Convert



Summary: $C(string_1) \xrightarrow{\text{converted}} C(string_2)$

The string of decimal characters of data type TN_1, sign and decimal type S_1 (S_1 = 00 is illegal), and scale factor 0 that starts at YC_1 is converted into a two's complement binary integer and stored, right justified, as a character string of length L_2 and starting location YC_2. If the string generated is longer than L_2, the high order excess is truncated and the overflow indicator is set. CN_2 shall be given in the 9-bit character format with legal codes of 000, 010, 100, 110. The length specified by L_2 shall be given as the number of 9-bit segments which make up the length of the binary number to be stored and shall be equal to or less than 8. Thus the stored binary number can be 9, 18, 27, 36, 45, 54, 63 or 72 bits long. The contents of $string_1$ remain unchanged.

Modifications: DU, DL are illegal for MF_1 and MF_2

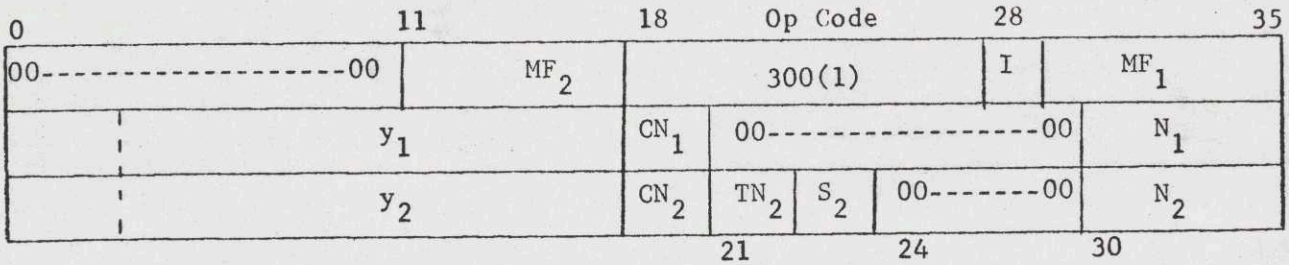
Indicators Affected:

Zero	If all the resultant bits generated were zero, then ON; otherwise OFF.
Negative	If the resultant sign is negative, then ON; otherwise OFF.
Overflow	If L_2 < string generated, then ON; otherwise unchanged.

Illegal Procedure Fault shall occur if DU or DL modifications are used for MF_1 or MF_2 or if any MBZ field in the multi-word instruction is non-zero, or if $L_2 > 8$, or if CN_2 does not contain a legal code, or if $S_1 = 00$.

3.4.4 Conversion Instructions (continued)

BTD Binary to Decimal Convert



Summary: C(string$_1$) $\xrightarrow{\text{converted}}$ C(string$_2$)

The two's complement binary integer starting at location YC_1 is converted into a signed string of decimal characters of data type TN_2, sign and decimal type S_2 (S_2 = 00 is illegal) and scale factor 0 and is stored, right justified, as a string of length L_2 starting at location YC_2. If the string generated is longer than L_2, the high order excess is truncated and the overflow indicator is set. The contents of string$_1$ remains unchanged. The length of string$_1$ (L_1) is given as the number of 9-bit segments which make up the bit string. L_1 shall be equal to or less than 8. Thus, the binary string to be converted can be 9, 18, 27, 36, 45, 54, 63 or 72 bits long. CN_1 designates a 9-bit character boundary.

Modifications: DU, DL, are illegal for MF_1 and MF_2.

Indicators Affected:

Zero	If the resultant number generated was zero, then ON; otherwise OFF.
Negative	If the resultant sign is negative, then ON; otherwise OFF.
Overflow	If $L_2 \leq$ string generated, then ON; otherwise unchanged.

Illegal Procedure Fault shall occur if DU or DL modifications are used for MF_1 or MF_2 or if any MBZ field of the multi-word instruction is non-zero, or if $L_1 > 8$, or if CN_1 does not contain a legal code, or if S_2 = 00.

3.4.8 Other Transfer Instructions

These two instructions provide additional transfer capability. Their format is the normal 600 general instruction format (with expanded Op Code field).

Mnemonic	Name of the Instruction	Op Code (octal)
TTN	Transfer on Tally Runout Indicator ON	606(1)

Summary: If Tally Runout Indicator ON, then Y ⟹ C(IC)

Modifications: All except DU, DL, CI, SC, SCR

Indicators Affected: None

Illegal Procedure fault shall occur for the following modifications: DU, DL, CI, SC, SCR

Mnemonic	Name of the Instruction	Op Code (Octal)
TPNZ	Transfer on Plus and Non-Zero	605(1)

Summary: If Negative Indicator OFF and Zero Indicator OFF, then Y ⟹ C(IC)

Modifications: All except DU, DL, CI, SC, SCR

Indicators Affected: None

Illegal Procedure Fault shall occur for the following modifications: DU, DL, CI, SC, SCR

Mnemonic	Name of the Instruction	Op Code (octal)
TMØZ	Transfer on Minus Or Zero	604(1)

Summary: If Negative Indicator ON or Zero Indicator ON, then Y ⟹ C(IC)

Modifications: All except DU, DL, CI, SC, SCR

Indicators Affected: None

Illegal Procedure Fault shall occur for the following modifications: DU, DL, CI, SC, SCR

3.13 MEASUREMENT AIDS

The 655/EIS Processor, like the 655 Processor, shall provide the capability to use a free-standing monitor to detect, record, and process selected system events. It should consequently not use the two op-codes set aside for future Monitor use.

3.14 PROCESSOR ID

To allow identification between various processor models and between models housed in EIS and pre-EIS processor cabinets, the following codes shall be read into bits 28-33 of the A register when an RSW instruction with an address $XXXXX2_8$ is executed (see 3.2.3 of the 655 Processor EPS-1).

Code	Processor Model
001000	6070
001001	6050
001011	6030
001100	6080
001101	6060
001111	6040